

TITLE 400G QSFP-DD FR4 Transceiver	DOC No. RFD-20220826006-002	
	REVISION : 01	AUTHORIZED BY : Andy Yang
	DATE : 2024.04.15	CLASSIFICATION : CONFIDENTIAL

1.Features

- Compliant with 400GBASE-FR4(IEEE802.3cu)
- Compliant with IEEE 802.3bs standard:
- 400GAUI-8 electrical interface
- Compliant with QSFP-DD MSA HW Rev 5.1
- type 2 housing with duplex LC connector
- Compliant with QSFP-DD CMIS Rev 5.0
- Maximum power consumption 9 W
- Case operating temperature 0°C to 70°C
- Two wire serial Interface with digital diagnostic monitoring
- Complies with EU Directive 2011/65/EU(RoHS compliant)
- Class 1 Laser

2.Production Description

2.1 Product Name and Series Numbers

400G QSFP-DD FR4 Transceiver

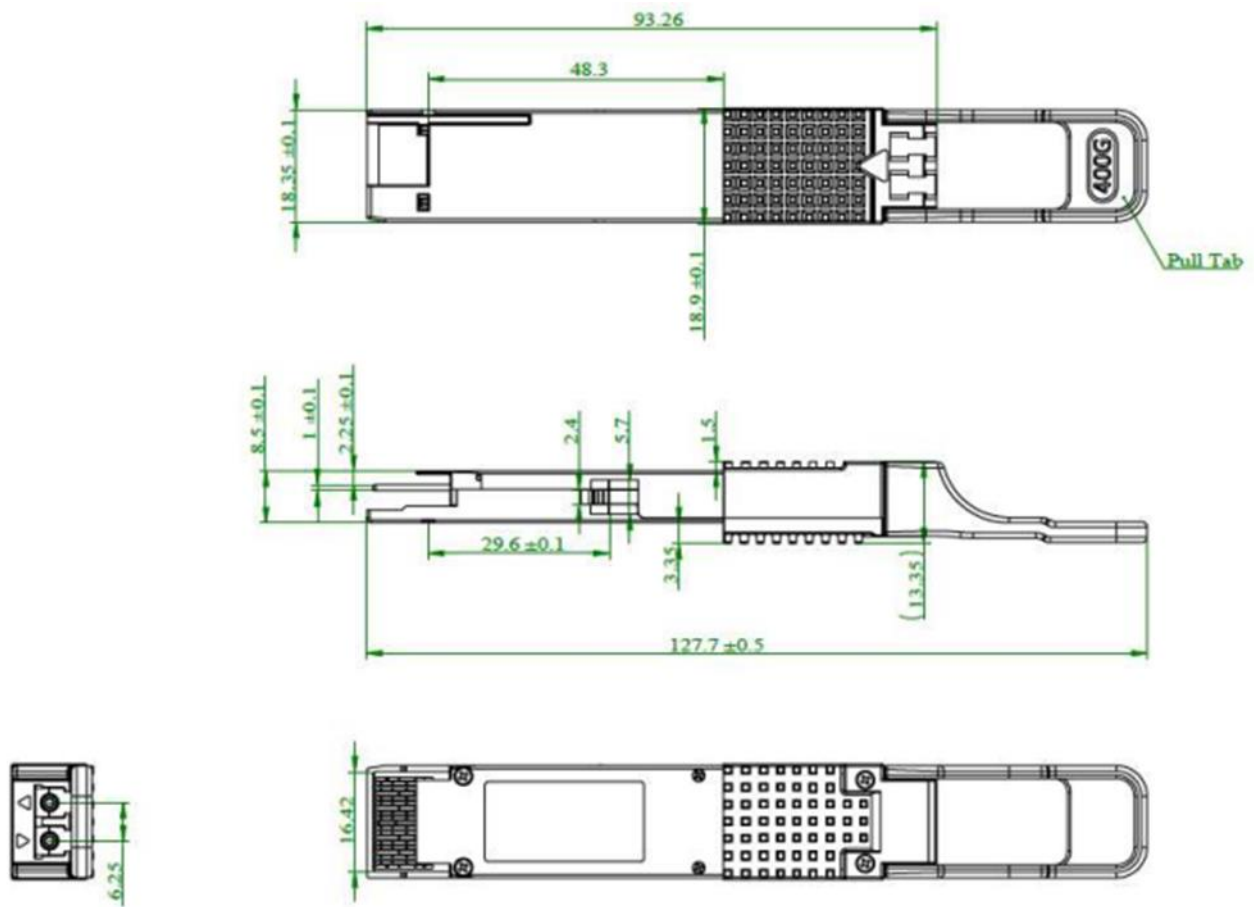
JPC P/N	Data Rate	Wavelength (nm)	Distance	Power (dBm)	Sen. (dBm)	Connector	Temp.
P66**9GRCK02-1	400G	CWDM	2km	-3.2~4.4	-4.6	LC	C

Note-1 : ** Indicates the customer code.

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2.2 Dimension, Materials, Plating and Marking

See the package outline for details.



Mechanical Package Outline (All dimensions in mm)

3.Product Specification

3.1 Absolute Maximum Ratings

Parameter	Symbol	Min.	Max.	Unit	Notes
Storage Temperature	T _s	-40	85	°C	
Supply Voltage	V _{CC}	-0.5	3.6	V	
Relative Humidity (non-condensing)	RH	5	95	%	

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Data Input Voltage Differential	$IV_{DIP-V_{DIN}}$	-	1	V	
Control Input Voltage	V_I	-0.3	$V_{CC}+0.5$	V	
Control Output Current	I_O	-20	20	mA	

3.2 Recommended Operating Conditions

Parameter	Symbol	Min.	Typical	Max.	Unit	Notes
Operating Case Temperature	T_{OPR}	0	-	70	°C	
Power Supply Voltage	V_{CC}	3.135	3.3	3.465	V	
Instantaneous peak current at hot plug	I_{CC_IP}	-	-	3600	mA	
Sustained peak current at hot plug	I_{CC_SP}	-	-	2970	mA	
Maximum Power Dissipation	P_D	-	-	9	W	
Maximum Power Dissipation, Low Power Mode	P_{DLP}	-	-	1.5	W	
Signalling Rate per Lane	SRL	-	53.125	-	Gbd	PAM4
Two Wire Serial Interface Clock Rate	-	-	-	400	kHz	
Module power supply noise tolerance 10 Hz - 10 MHz (ptp)	-	-	-	66	mVpp	
Rx Differential Data Output Load	-	-	100	-	Ohm	
Operating Distance	-	2	-	2000	m	

3.3 Transmitter Optical Specifications

Parameter	Symbol	Min.	Typical	Max.	Unit	Notes
Wavelength L0	λ_{C0}	1264.5	1271	1277.5	nm	
Wavelength L1	λ_{C1}	1284.5	1291	1297.5	nm	
Wavelength L2	λ_{C2}	1304.5	1311	1317.5	nm	
Wavelength L3	λ_{C3}	1324.5	1331	1337.5	nm	
Side Mode Suppression Ratio	SMSR	30	-	-	dB	
Average Launch Power, each lane	AOP_L	-3.2	-	4.4	dBm	1
Outer Optical Modulation Amplitude (OMA_{outer}), each lane	T_{OMA}	-	-	3.7	dBm	
Outer Optical Modulation Amplitude (OMA_{outer}) each lane: for TDECQ <1.4dB for 1.4 ≤ TDECQ = 3.4dB	T_{OMA}	-0.2 -1.6+TDECQ				
Difference in launch power between any two lanes (OMA_{outer})	DP	-	-	3.9	dB	
Transmitter and Dispersion Eye Closure for PAM4 (TDECQ), each lane	TDECQ	-	-	3.4	dB	
Transmitter eye closure for PAM4(TECQ)	TECQ	-	-	3.4	dB	
TDECQ - TECQ	-	-	-	2.5	dB	

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Over/under-shoot	-	-	-	22	%	
Transmitter power excursion	-	-	-	1.8	dBm	
Average Launch Power of OFF Transmitter, each lane	T_{OFF}	-	-	-16	dBm	
Extinction Ratio, each lane	ER	3.5	-	-	dB	
Transmitter transition time	-	-	-	17	ps	
$RIN_{17.1OMA}$	RIN	-	-	-136	dB/Hz	
Optical Return Loss Tolerance	ORL	-	-	17.1	dB	
Transmitter Reflectance	T_R	-	-	-26	dB	

Note 1: Average launch power, each lane (min) is informative and not the principal indicator of signal strength.

3.4 Receiver Optical Specifications

Parameter	Symbol	Min.	Typical	Max.	Unit	Notes
Wavelength L0	λ_{C0}	1264.5	1271	1277.5	nm	
Wavelength L1	λ_{C1}	1284.5	1291	1297.5	nm	
Wavelength L2	λ_{C2}	1304.5	1311	1317.5	nm	
Wavelength L3	λ_{C3}	1324.5	1331	1337.5	nm	
Damage Threshold, each lane	AOP_D	5.4	-	-	dBm	
Average Receive Power, each lane	AOP_R	-7.2	-	4.4	dBm	1
Receive Power (OMA_{outer}), each lane	OMA_R	-	-	3.7	dBm	
Difference in receive power between any two lanes (OMA_{outer})	DR	-	-	4.1	dB	
Receiver Reflectance	RR	-	-	-26	dB	
Receiver Sensitivity (OMA_{outer}), each lane for $TECQ < 1.4dB$ for $1.4 = TECQ = 3.4dB$	S_{OMA}	-	-	-4.6 -6+TECQ	dBm	
Stressed Receiver Sensitivity (OMA_{outer}), each lane	SRS	-	-	-2.6	dBm	
Conditions of stressed receiver sensitivity test						
Stressed eye closure for PAM4 (SECQ)	-	-	3.4	-	dB	
OMA_{outer} of each aggressor lane	-	-	1.4	-	dBm	

Note 1: Average receive power, each lane (min) is informative and not the principal indicator of signal strength.

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3.5 Electrical Specification High Speed Signal (compliant with IEEE 802.3bs 400GAUI-8)

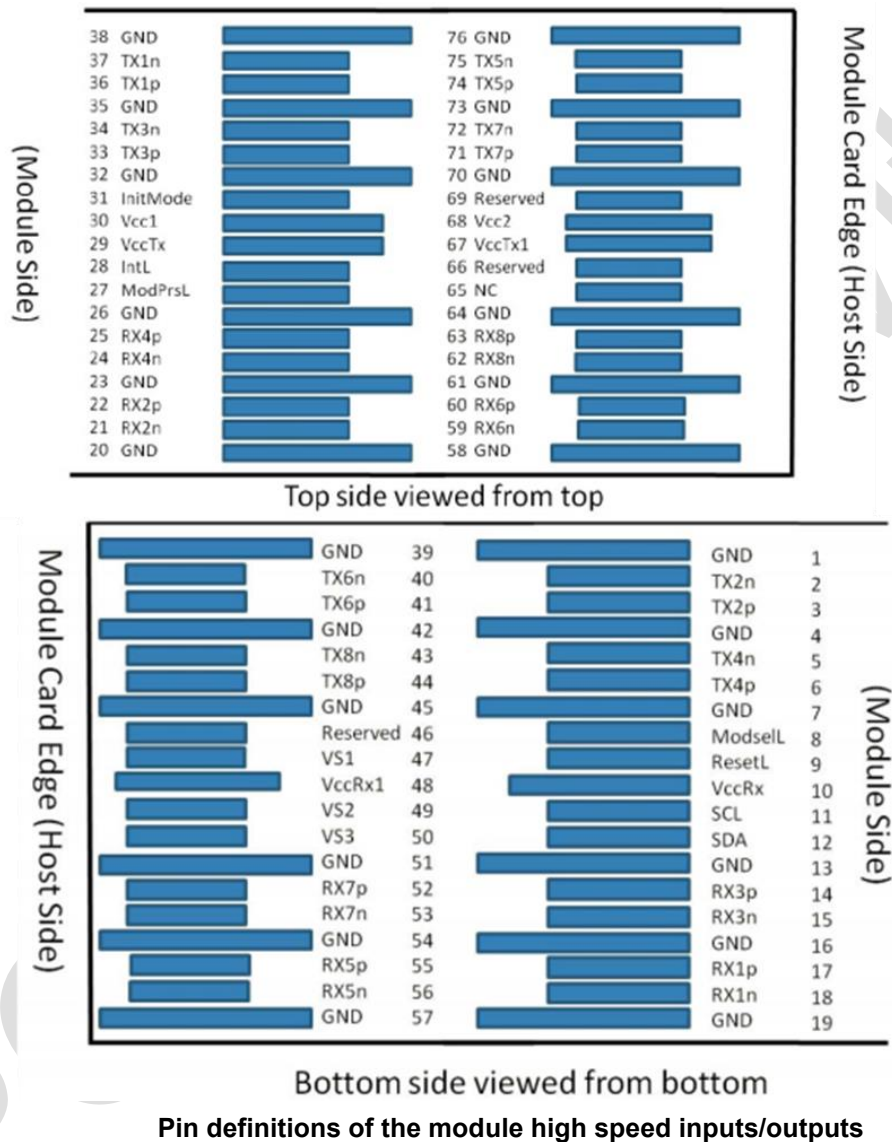
Receiver (Module Output)						
Parameter	Symbol	Min.	Typical	Max.	Unit	Notes
AC common-mode output Voltage (RMS)		-	-	17.5	mV	
Differential output Voltage		-	-	900	mV	
Near-end Eye height, differential		70	-	-	mV	
Far-end Eye height, differential		30	-	-	mV	
Far end pre-cursor ISI ratio		-4.5	-	2.5	%	
Differential Termination Mismatch		-	-	10	%	
Transition Time (min, 20% to 80%)		9.5	-	-	ps	
DC common mode Voltage		-350	-	2850	mV	
Transmitter (Module Input)						
Parameter	Symbol	Min.	Typical	Max.	Unit	Notes
Differential pk-pk input Voltage tolerance		900	-	-	mV	
Differential termination mismatch		-	-	10	%	
Single-ended voltage tolerance range		-0.4	-	3.3	V	
DC common mode Voltage		-350	-	2850	mV	

3.6 Electrical Specification Low Speed Signal (compliant with QSFP-DD HW Rev 5.1)

Parameter	Symbol	Min.	Max.	Unit	Condition
Module output SCL and SDA	V _{OL}	0	0.4	V	
Module Input SCL and SDA	V _{IL}	-0.3	V _{CC} *0.3	V	
	V _{IH}	V _{CC} *0.7	V _{CC} +0.5	V	
LPMode, ResetL, ModSelL and ePPS	V _{IL}	-0.3	0.8	V	
	V _{IH}	2	V _{CC} +0.3	V	
IntL	V _{OL}	0	0.4	V	
	V _{OH}	V _{CC} -0.5	V _{CC} +0.3	V	

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6.Pin Assignments



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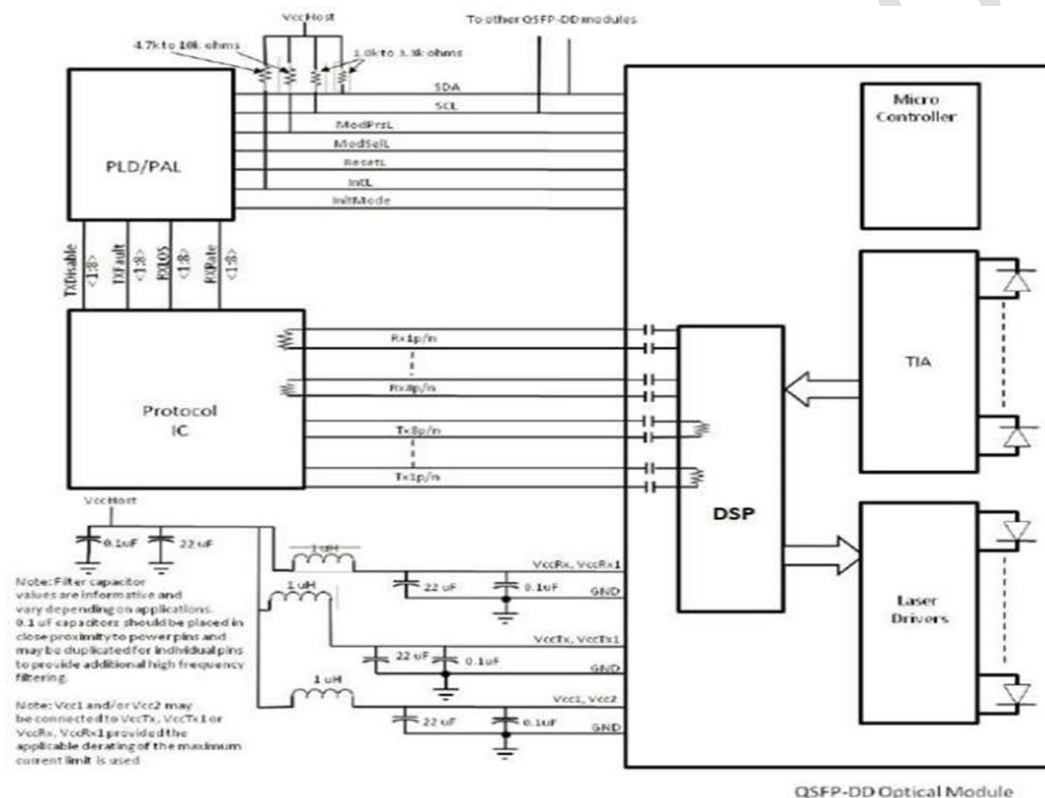
Electrical Pin Definition

Pin #	Logic	Symbol	Definition	Pin #	Logic	Symbol	Definition
1		GND	Ground	39		GND	Ground
2	CML-I	Tx2n	Transmitter Inverted Data Input	40	CML-I	Tx6n	Transmitter Inverted Data Input
3	CML-I	Tx2p	Transmitter Non-inverted Data Input	41	CML-I	Tx6p	Transmitter Non-inverted Data Input
4		GND	Ground	42		GND	Ground
5	CML-I	Tx4n	Transmitter Inverted Data Input	43	CML-I	Tx8n	Transmitter Inverted Data Input
6	CML-I	Tx4p	Transmitter Non-inverted Data Input	44	CML-I	Tx8p	Transmitter Non-inverted Data Input
7		GND	Ground	45		GND	Ground
8	LVTTL-I	ModSelL	Module Select	46		Reserved	
9	LVTTL-I	ResetL	Module Reset	47		VS1	Module Vendor Specific 1
10		VccRx	+3.3V Power Supply Receiver	48		VccRx1	3.3V Power Supply
11	LVCMS - I/O	SCL	2-wire serial interface clock	49		VS2	Module Vendor Specific 2
12	LVCMS - I/O	SDA	2-wire serial interface data	50		VS3	Module Vendor Specific 3
13		GND	Ground	51		GND	Ground
14	CML-O	Rx3p	Receiver Non-inverted Data Output	52	CML-O	Rx7p	Receiver Non-inverted Data Output
15	CML-O	Rx3n	Receiver Inverted Data Output	53	CML-O	Rx7n	Receiver Inverted Data Output
16		GND	Ground	54		GND	Ground
17	CML-O	Rx1p	Receiver Non-inverted Data Output	55	CML-O	Rx5p	Receiver Non-inverted Data Output
18	CML-O	Rx1n	Receiver Inverted Data Output	56	CML-O	Rx5n	Receiver Inverted Data Output
19		GND	Ground	57		GND	Ground
20		GND	Ground	58		GND	Ground
21	CML-O	Rx2n	Receiver Inverted Data Output	59	CML-O	Rx6n	Receiver Inverted Data Output
22	CML-O	Rx2p	Receiver Non-inverted Data Output	60	CML-O	Rx6p	Receiver Non-inverted Data Output
23		GND	Ground	61		GND	Ground
24	CML-O	Rx4n	Receiver Inverted Data Output	62	CML-O	Rx8n	Receiver Inverted Data Output
25	CML-O	Rx4p	Receiver Non-inverted Data Output	63	CML-O	Rx8p	Receiver Non-inverted Data Output
26		GND	Ground	64		GND	Ground
27	LVTTL-O	ModPrsL	Module Present	65		NC	Not connected
28	LVTTL-O	IntL	Interrupt	66		Reserved	
29		VccTx	+3.3V Power Supply Transmitter	67		VccTx1	3.3V Power Supply

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30		Vcc1	+3.3V Power Supply	68		Vcc2	3.3V Power Supply
31	LVTTL-I	InitMode	Initialization mode	69		Reserved	
32		GND	Ground	70		GND	Ground
33	CML-I	Tx3p	Transmitter Non-inverted Data Input	71	CML-I	Tx7p	Transmitter Non-inverted Data Input
34	CML-I	Tx3n	Transmitter Inverted Data Input	72	CML-I	Tx7n	Transmitter Inverted Data Input
35		GND	Ground	73		GND	Ground
36	CML-I	Tx1p	Transmitter Non-inverted Data Input	74	CML-I	Tx5p	Transmitter Non-inverted Data Input
37	CML-I	Tx1n	Transmitter Inverted Data Input	75	CML-I	Tx5n	Transmitter Inverted Data Input
38		GND	Ground	76		GND	Ground

Recommended QSFP-DD Host Board Schematic



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Digital Diagnostics Monitor

Parameter	Range	Accuracy	Unit	Calibration
Temperature	0 to 70	±3	°C	Internal
Voltage	0 to V _{CC}	0.1	V	Internal
Tx Bias Current (Each Lane)	0 to 100	10%	mA	Internal
Tx Output Power (Each Lane)	-3.2 to +4.4	±3	dB	Internal
Rx Receive Power (Each Lane)	-7.2 to +4.4	±3	dB	Internal

7.Modification History

Rev.	Comments	Date	Originator	Approval
01	Preliminary Draft	2024.04.15	Andy Yang	Mike Sun